

PTO-1449 REPRODUCED  <b>INFORMATION DISCLOSURE CITATION IN AN APPLICATION</b>  (06-16-00)  (Use several sheets if necessary)		ATTORNEY DOCKET NO. 2789.2001-001  APPLICATION NO. 09/557,640  APPLICANT William J. Dally et al.  FILING DATE 04/25/00  GROUP				
<b>U.S. PATENT DOCUMENTS</b>						
EXAM- INER INI- TIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE IF APPROPRIATE
	AA					
	AB					
	AC					
	AD					
	AE					
	AF					
	AG					
	AH					
	AI					
	AJ					
	AK					
<b>FOREIGN PATENT DOCUMENTS</b>						
	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION YES NO
	AL					
	AM					
	AN					
<b>OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)</b>						
JT	AR	Dally, William J. and Poulton, John W., <i>Digital Systems Engineering</i> , Cambridge University Press, 1998, pp. 428-447, 537-540 and 547-548.				
TT	AS	Kim, Weigant and Gray, "PLL/DLL System Noise Analysis for Low Jitter Clock Synthesizer Design," <i>ISCAS</i> , 1994, pp. 31-34.				
TT	AT	Waizman, A., "A Delay Line Loop for Frequency Synthesis of De-Skewed Clock," <i>IEEE International Solid-State Circuits Conference</i> , 1994, pp. 298-299.				
TT	AU	Dally, William J. and Poulton, John W., "Transmitter Equalization for 4Gb/s Signaling," <i>IEEE Micro</i> , Jan-Feb 1997, pp. 48-56.				
EXAMINER			DATE CONSIDERED			
			<div style="font-size: 1.5em; font-family: cursive;">09/01/03</div>			